Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A processor comprising:

a first memory to store instructions and data for use by the processor, the first memory further to store data representing a first state of a cellular automaton at a first time step, the data to be organized in cells;

a first update engine, the first update engine including a microprocessor execution unit capable of executing general purpose microprocessor instructions;

a cellular automaton prefetch state machine to prefetch data from cells to be updated and associated neighborhood cells and store the prefetched data in a neighborhood buffer; and

a cellular automaton update unit to provide data from ~~selected cells of the cellular automaton~~ the neighborhood buffer to the first update engine,

the first update engine to update at least some of the selected cells according to an update rule and a state of any associated neighborhood cells to provide a state of the cellular automaton at a second time step, the first memory, the cellular automaton prefetch state machine, the neighborhood buffer, the first update engine and the cellular automaton update unit being integrated on a single micro-processor chip.

2. (Canceled)

3. (Currently Amended) The processor of claim [[2]] 1 wherein the cellular automaton prefetch state machine is further to write data representing the second state of the cellular automaton back to the first memory.

4. (Currently Amended) The processor of claim [[2]] 1 further comprising:

data rasterizer control circuitry, the data rasterizer control circuitry, together with the cellular automaton prefetch state machine to rasterize prefetched data to be stored in the neighborhood buffer.

5. (Canceled)

6. (Currently Amended) The processor of claim [[5]] 1 wherein the first memory comprises a first cache memory and the neighborhood buffer comprises a second cache memory.

7. (Currently Amended) The processor of claim [[5]] 1 wherein the neighborhood buffer comprises a cache line buffer.

8. (Currently Amended) The processor of claim [[5]] further comprising:

shifter logic to select from the neighborhood buffer a cell to be updated and associated neighborhood cells, the shifter logic further to present data associated with the selected cells to the update engine.

9. (Original) The processor of claim 1 further comprising:

a second update engine, wherein the first and second update engines are pipelined, the first update engine to update the cellular automaton to provide the second state of the cellular automaton at the second time step, the second update engine to update the second state of the cellular automaton to provide a third state of the cellular automaton at a third time step.

10. (Currently Amended) The processor of claim 9 ~~further comprising:~~

wherein ~~a cellular automaton prefetch state machine,~~ the cellular automaton prefetch state machine is further to write data representing the third state of the cellular automaton back to the first memory.

11. (Currently Amended) A microprocessor comprising:

a cache memory hierarchy including at least two levels of cache memory, a first level of the cache memory to store data representing a first state of a cellular automaton at a first time step, the data being organized in cells and a second level of the cache memory to receive prefetched, rasterized cellular automaton data;

an execution cluster including at least a first execution unit to execute microprocessor instructions; and

a cellular automaton update unit, the cellular automaton update unit to provide data ~~associated with cells of the cellular automaton~~ from the second level of the cache memory to the first execution unit, the first execution unit to update each cell to be updated in the cellular automaton in response to an update rule and in response to a state of any associated neighborhood cells at the first time step to provide a second state of the cellular automaton at a second time step.

12. (Previously Presented) The microprocessor of claim 11 wherein the execution cluster further comprises at least a second execution unit, the first and second execution units being pipelined, the second execution unit to update each cell of the cellular automaton at the second time step to provide a third state of the cellular automaton at a third time step such that the cellular automaton is updated at least twice before associated data is written back to the first level of the cache memory hierarchy.

13. (Original) The microprocessor of claim 12 wherein the cellular automaton update unit comprises:

data rasterizer control circuitry, the data rasterizer control circuitry in conjunction with a prefetch state machine to rasterize data associated with the cellular automaton cells to be provided to the first execution unit, and

one or more shifters, the one or more shifters to shift the rasterized data past the first execution unit and to shift data associated with the second state of the cellular automaton past the second execution unit.

14. (Original) The microprocessor of claim 13 wherein the cellular automaton update unit further comprises:

a data store to store data associated with a cell at the second time step and all associated neighborhood cells until all the associated neighborhood cells have been updated by the first execution engine.

15. (Original) The microprocessor of claim 11 further comprising:

a prefetch state machine, the prefetch state machine to prefetch data associated with the cell to be updated and associated neighborhood cells.

16. (Original) The microprocessor of claim 15 wherein the cellular automaton update unit comprises:

data rasterizer control circuitry, the data rasterizer control circuitry in conjunction with the prefetch state machine to rasterize prefetched data to be provided to the first execution unit.

17. (Currently Amended) The microprocessor of claim 16 wherein the cellular automaton update unit further comprises:

one or more shifters to shift the rasterized data stored in the second level cache memory past the first execution unit.

18. (Original) The microprocessor of claim 11 further including a microcode read-only memory, the microcode read only memory to include microcode to support at least one cellular automaton-specific operation.

19. (Currently Amended) A method comprising:

storing data representing a state of a cellular automaton at a first time step in a first memory of a general-purpose processor;

prefetching a portion of the stored data;

rasterizing [[a]] the portion of the stored data, the portion including at least data associated with a cell to be updated and associated neighborhood cells;

storing the prefetched rasterized data in second neighborhood memory;

updating the cell to be updated according to an update rule and a state of the associated neighborhood cells at the first time step, at least a portion of the updating to be performed by a microprocessor execution unit capable of executing general-purpose microprocessor instructions; and

repeating prefetching, rasterizing, storing and updating until all cells to be updated have been updated such that a state of a cellular automaton at a second time step is provided, the rasterizing and updating to be performed by circuitry on a same chip as the memory.

20. (Original) The method of claim 19 further comprising:

writing back to the memory data representing the updated state of the cellular automaton.

21. (Previously Presented) The method of claim 20 further comprising:

repeating rasterizing and updating until all cells to be updated have been updated at least twice prior to writing back to the memory.

22. (Currently Amended) A system comprising:

a bus to communicate information;

a device coupled to the bus to enable access to a medium storing an application including a cellular automaton; and

a ~~general-purpose~~ micro-processor capable of executing general-purpose instructions coupled to the bus to execute the application, the ~~general-purpose~~ micro-processor including:

a memory to store data representing a state of the cellular automaton at a first time step, the data being organized in cells,

a cellular automaton prefetch state machine to control prefetching of data to be provided to the execution unit and wherein,

the memory is a first on-chip cache memory, the processor further including a second on-chip cache memory to store the prefetched data,

an execution cluster including a first execution unit, the first execution unit capable of executing at least some general-purpose microprocessor instructions; and

a cellular automaton update unit to provide data associated with cells of the cellular automaton to the first execution unit, the first execution unit to update each cell to be updated in the cellular automaton in response to an update rule and in response to a state of any associated neighborhood cells at the first time step to provide a second state of the cellular automaton at a second time step.

23. (Original) The system of claim 22 wherein the device is a mass storage unit.

24. (Original) The system of claim 22 wherein the device is a network connection device.

25. (Canceled)

26. (Currently Amended) The system of claim [[25]] 22 wherein the cellular automaton prefetch state machine is further to write data representing the state of the cellular automaton at the second time step back to the memory.

27. (Original) The system of claim 22 wherein the memory is an on-processor cache memory.

28. (Canceled)

29. (Previously Presented) The system of claim 22 wherein the processor further includes

a second execution unit pipelined with the first execution unit, the second execution unit to update each cell to be updated in the second state of the cellular automaton to provide a third state of the cellular automaton at a third time step before an updated state is written back to the memory.